INTERN SCHOLARS

The Semiconductor Research Corporation (SRC) Education Alliance and GLOBALFOUNDRIES are pleased to announce a special internship opportunity for SRC graduate students. Selected Intern Scholars will pursue innovative research in semiconductor manufacturing at GLOBALFOUNDRIES’ state-of-the-art facilities. Please see below for a detailed description of available internship positions.

Eligibility: Ph.D., M.S. students currently supported by SRC or the SRC Education Alliance are eligible for the Intern Scholars program.

Application: Applicants must reply by email to apply@src.org with position number and job title(s) of interest, please include a current CV. One submission may list multiple jobs. No cover letter necessary. Submissions must be received no later than February 16, 2016.

Selection: Selection is based on evaluation by SRCEA committee members on a rolling basis. Intern Scholar assignments are for 10 weeks and selected Intern Scholars will receive a competitive stipend commensurate with experience.

Open Positions:

01_SRCEA: Spin Transfer Torque Memory Devices, Malta, NY
02_SRCEA: System-level Monolithic 3D IC Design using GLOBALFOUNDRIES 22nm and 14nm production PDKs, Santa Clara, CA
03_SRCEA: 3D Sensor Network Design, Malta, NY
04_SRCEA: End-to-End Statistical Data Analysis for Product Quality & Cost Improvement, Burlington, VT
05_SRCEA: Test & Characterization Engineer to work on development of novel embedded non-volatile memory, East Fishkill, NY
06_SRCEA: Noise Analysis for High-Performance Analog Circuit Design, Raleigh, NC
07_SRCEA: Analog Design and simulation of High Speed SerDes Link (HSS) Analog building blocks, Burlington, VT
08_SRCEA: 56Gb/s Serializer/DeSerializer Verification and Modeling Enhancement, East Fishkill, NY
09_SRCEA: Computational DSA (directed self-assembly) GLOBALFOUNDRIES-SRCEA internship, Santa Clara, CA
10_SRCEA: mmWave Circuit Design in 22nm FDSOI Technology, Austin, TX
11_SRCEA: Explore and evaluate the transport behavior in advanced high mobility materials and its implication in advanced CMOS technology, Malta, NY

12_SRCEA: Explore and evaluate the parasitic resistance and capacitance in the advanced CMOS nodes and its implication to technology performance, Malta, NY

13_SRCEA: 3D RF Simulation and Optimization of Inductor Designs for 14nm RF Platform Malta NY

14_SRCEA: Monte Carlo simulation/close-formed analysis on RC performance for foundational BEOL (Back End of Line) process assumptions for 10nm/7nm technology nodes, Malta, NY
Job Summary:

The candidate will support TD Research organization’s differentiating solutions group by performing power-performance-area (PPA) analysis of novel STT-MRAM devices.

Specific Responsibilities Include:

The intern will be responsible to work with Differentiating solutions group to understand and benchmark scaled STT MRAM devices through analytical methods and circuit benchmarking techniques. The intern will have the opportunity to understand, correlate and benchmark scaled logic and memory technology nodes. The intern is expected to make relevant presentations & publications within and outside the research groups. The intern is also expected to write technical reports and present key findings.

Required Qualifications:

- Graduate student, pursuing degree in Electrical Engineering
- Understanding physics of magnetic materials and devices such as spin transfer torque effect, spin orbit coupling effects, spin hall effect etc.
- Understanding scaled CMOS technology
- Understand power-performance-area scaling of CMOS and non-CMOS devices

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The candidate will use industry standard system-level 2D IP and will partition it into monolithic 3D IC. After placement, routing, and timing closure, the candidate will extract Power/Performance/Area (PPA) from the 3D layout and compare it with 2D IC.

Specific Responsibilities Include:

- Partitioning of one-tier 2D IC to two-tier monolithic 3D IC
- Complete RTL to GDSII placement, routing, and parasitic extraction from the layout
- Calculate PPA (power, performance, area) of Monolithic 3D IC compared to that of standard 2D IC
- Access to advanced manufacturing PDK (22nm and 14nm CMOS technologies)

Required Qualifications:

- Pursuing graduate degree in Electrical Engineering, Computer Science, Computer Engineering, 2nd or 3rd year student
- Experience with IC design, use for design EDA tools for synthesis, place & route, timing, parasitic extraction, and Hspice

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The objective of the internship project is to design and validate sensor networks to monitor the IR droop in power delivery network and timing delay in digital circuits.

Specific Responsibilities Include:

The intern will work directly with advanced circuit design, packaging, and characterization test engineers to access the necessary design manuals, develop sensor networks and characterize them for 14nm technology.

The intern will also conduct the necessary theoretical computation, verify it through circuit-level and system-level simulations, and help in transferring the design to standard cell by interfacing with the layout engineer.

The intern will have the opportunity to learn about hardware design, verification, tapeout and inline tests to characterize the circuits and package test for functional validation.

More specifically, the assignment would involve interfacing with the memory solutions and advanced circuit design teams to understand the power delivery network for SRAM. Additionally, develop standard cells for the IR droop and delay sensors through layout reviews and running DRC and FabDRC checks will be another facet. The intern will participate in troubleshooting efforts as needed and help to develop permanent solutions. Lastly, the intern will support in technology transfer efforts from the other GLOBALFOUNDRIES facilities.

Required Qualifications:

- Pursuing graduate degree in Electrical Engineering or Computer Engineering, 2nd or 3rd year student

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The candidate will perform statistical data analysis of End-to-End test results. We will collaborate with a key client to merge their test results for a 32nm ASIC with our internal wafer & final test results. The program objective is to evaluate correlations between client card & system failures -- with internal test results. Ideally we will develop recommendations for testing process improvements and will improve yield, cost and quality.

Specific Responsibilities Include:

The Intern will be responsible for data correlation analysis. (A deep knowledge of statistics is preferred, but not required).

The Intern will work with test teams both within GLOBALFOUNDRIES and a key client to understand the testing process and data elements.

The intern will learn the details of the wafer probe and Final Test process for semiconductors working with engineers from Test Engineering, Design-for-Test, Customer Quality and Product Engineering.

Required Qualifications:

- Pursuing graduate degree in Electrical Engineering, Computer Science, Computer Engineering, 2nd or 3rd year student

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
05_SRCEA: Test & Characterization Engineer to work on development of novel embedded non-volatile memory, East Fishkill, NY

Job Summary:

The objective of the internship project is to characterize and test both device and functional macros for embedded multi-time programmable non-volatile memory in 14LPP 2D/3D technology. The candidate will write test plans, and execute tests on wafer and packaged parts to measure macros and feedback learning to the design and integration teams. The candidate will perform statistical data analysis of offline and inline data. The intern will work directly with advanced non-volatile memory designers; packaging and characterization test engineers to access the necessary data.

Specific Responsibilities Include:

The intern will be responsible for characterization of multi-time programmable device and functional macros in 14nm technology.

The intern will develop test code and plans for device and functional macro validation and statistical data gathering. The intern will have the opportunity to learn about device and functional macro design, design verification, device to functional macro correlation, test coding of functional ATE and parametric analyzers.

The intern will have the opportunity to learn about device and functional macro design in 14LPP technology, design verification techniques, device to functional macro correlation, statistical data analysis techniques used in semiconductor industry, test coding of functional ATE and parametric analyzers.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical Engineering, 2nd or 3rd year student preferred.

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
06_SRCEA: Noise Analysis for High-Performance Analog Circuit Design, Raleigh, NC

Job Summary:

The candidate will work with our experienced high-speed analog circuit designers to analyze the effects of noise in an on-chip environment in the context of GLOBALFOUNDRIES’ world-leading SerDes designs.

Specific Responsibilities Include:

The intern will be responsible for developing a means to analyze noise effects on circuits and signal jitter and develop mitigation techniques in partnership with the larger team.

The intern will develop simulation strategies to model noise effects on analog circuits and then propose solutions. The opportunity exists to create novel solutions to these problems and the potential for doing an invention disclosure and/or paper in this burgeoning field is recognized.

The intern will have the opportunity to work on cutting-edge SerDes design at 30Gb/s and 56Gb/s on the most advanced process nodes in the industry. The candidate can expect to work under the leadership of a Distinguished Member of the Technical Staff and other senior level engineers as both mentors and colleagues. Skills in simulation, physical design, and manufacturability techniques will be developed with an emphasis on real-world product design skills.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical Engineering 2nd, 3rd or 4th year student preferred.
- Familiarity with Cadence design infrastructure (Virtuoso schematic capture, Spectre simulation)

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
07_SRCEA: Analog Design and simulation of High Speed SerDes Link (HSS) Analog building blocks, Burlington, VT

Job Summary:

Analog Design and simulation of High Speed SerDes Link (HSS) Analog building blocks. The candidate will work with the world's leading HSS design team to learn and apply advanced Analog design and simulation techniques on next generation HSS designs. Candidate would be paired with a senior level mentor working with diverse team to optimize learning and application.

Specific Responsibilities Include:

The candidate will be responsible for design and analysis of HSS Analog circuit building blocks. Reviewing results and improving the circuit performance to meet design specifications.

Candidate assignment will involve detailed circuit design, simulation and results analysis utilizing Cadence schematic capture and Spectre simulation.

The results of these design and simulation efforts will be reviewed by the HSS team members and feedback provided. The ultimate goal being a circuit block which would be incorporated into the larger HSS design. Additional opportunities to perform layout based parasitic extraction simulation and performance analysis as well. The ultimate goal is a production ready design which meets performance specifications across manufacturing process corners.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical & Computer Engineering, 2nd year student preferred.
- Familiarity in schematic layout a plus

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The candidate would get the opportunity to work on world leading IP and contribute to our next product, as well as improve our design verification process. Our team is enhancing our SerDes verification to create a verification bridge between the MatLab/C modeling environment and our System Verilog verification environment. We are developing our SerDes architecture using Matlab and C to create a golden model that also gets delivered to the customer. As we develop this architecture, we need a path to correlate this golden model against the hardware design. The goal of this internship is to create a bridge between these two environment to to enable correlation of the model to the final design.

Specific Responsibilities Include:

The intern will be responsible for investigating and develop the bridge between the MatLab & C models to run the final design within the SystemVerilog (SV) / Universal Verification Methodology (UVM) to enable verification of our final 56Gb/s SerDes.

The intern will be responsible for understanding and writing test cases within the UVM environment as a basis to incorporate in the matlab/C model.

The intern will have the opportunity to work with a State-of-Art SerDes design team and learn about the development and architecture of the most advanced designs in the world.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical or Computer Engineering or Computer Science, 2nd - 3rd year student preferred.
- Skills required include a strong logic design familiarity with VHDL or Verilog as well as MatLab and C programming

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

This intern is responsible for conducting algorithm development and/or simulation studies for the DSA (directed self-assembly) project in GLOBALFOUNDRIES.

Specific Responsibilities Include:

The intern will be responsible for learning, using and upgrading the presently available GLOBALFOUNDRIES DSA simulation tools, conducting parametric DSA simulation studies, documenting and presenting the results.

The intern will utilize rigorous and/or compact models to investigate the effects of DSA fluctuations and ways to mitigate those effects, and develop code to incorporate the fluctuation effect assessment functionality into our DSA solver. Further, the intern will develop a method to calculate and visualize process variability bands associated with those fluctuations.

The intern will have an opportunity to contribute to an industry-relevant research project, and interact directly with senior R&D Engineering staff and management to provide support in the above activities.

Required Qualifications:

- Pursuing graduate degree majoring in Computer Engineering, Physics or Mathematics; 2nd, 3rd or 4th year student preferred.

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The intern will be helping the RF design enablement team to explore ideas on the design of mmWave circuits which are of interest to GF's customers.

Specific Responsibilities Include:

The intern will design schematic, simulate and layout the mmWave circuits. He/She will also try different layout techniques which is very critical for mmWave circuits. The intern will also be responsible for extracting and running post-layout simulations.

The intern has to develop some methodology for designing mmWave circuits.

Finally the intern has to link the critical process/device parameters for the 22nm FDSOI process to the mmWave circuit parameters to be developed.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical Engineering, 2nd, 3rd year student preferred.

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

This position is for Summer Internship working with GLOBALFOUNDRIES' Advanced Technology Development Device Engineering Department at Malta, NY. The candidate will closely work with ATD device and integration as well as TCAD team to explore and evaluate the transport behavior in advanced high mobility materials and its implication in advanced CMOS technology. In particular, the successful applicant will perform research on quantifying and modeling the transport mechanism in the device with novel channel materials.

Specific Responsibilities Include:

- Responsible for evaluation of the device design trade-off between different channel materials in advanced CMOS technology nodes
- Identify opportunities to improve device performance in the advanced technology node.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical Engineering, 2nd, 3rd or 4th year student preferred.
- Knowledge of CMOS Scaling
- Familiarity with semiconductor manufacturing and chip design.
- Familiarity with TCAD simulation tool

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
12_SRCEA: Explore and evaluate the parasitic resistance and capacitance in the advanced CMOS nodes and its implication to technology performance, Malta, NY

Job Summary:

This position is for Summer Internship working with GLOBALFOUNDRIES' Advanced Technology Development Device Engineering Department at Malta, NY. The candidate will closely work with ATD device and integration as well as TCAD team to explore and evaluate the parasitic resistance and capacitance in the advanced CMOS nodes and its implication to technology performance. In particular, the successful applicant will perform research on quantifying and modeling the parasitic resistance and capacitance in different MOL integration scheme and metallurgical material.

Specific Responsibilities Include:

- Responsible for evaluation of the device design trade-off between different MOL integration scheme and metallurgical contact materials in advanced CMOS technology nodes
- Identify opportunities to improve device performance in the advanced technology node.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical Engineering, 2nd, 3rd or 4th year student preferred.
- Knowledge of CMOS Scaling

Additional Qualifications:

- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
On-Chip Inductors are becoming very attractive and cost effective option for the Radio Frequency Integrated Circuits (RF ICs) due to simple realizations on the CMOS backend stack metal layers. All major RF IC components (low noise amplifiers (LNAs), oscillators, filters, baluns, matching networks and mixers) in a narrowband front-end system need inductors and transformers.

The simulation work is around the optimization of Inductors designs for 14nm RF platform using 3D simulators. The self and mutual inductances of a variety of geometries to be optimized to suit the general purpose customers need. New process and design methods are to be investigated to improve Inductors RF performance beyond the standard offerings. A particular attention is to be paid to geometries that approximate a square and circular spiral, permitting simple, and accurate expressions

The candidate will learn about the 14nm FinFET process, Inductors designs and RF simulations software. Candidate will run the RF simulations of various designs and compare with the platform results. He will optimized the Inductor designs and simulations methods.

Specific Responsibilities Include:
- Running Simulations - candidate will use the Sonnet 3D software to investigate the design of Inductors.
- Inductor design optimization; substrate loss, number of turns and process parameters
- Candidate will carry on the design work to further improve the RF performance of the devices.
- Electromagnetic theory, and mathematical calculations.

Required Qualifications:
- Pursuing graduate degree majoring in Electrical or Computer Engineering or Physics, 2nd - 3rd year student preferred.
- Familiarity of Electromagnetic theory, Physics, and Simulations

Additional Qualifications:
- Strong communication skills
- Collaboration / teamwork
- Adaptability & flexibility
- Good problem solving and knowledge of experimental methods
- Planning & organization / able to drive and execute projects/work
Job Summary:

The candidate will support improvement to the foundational Back End of Line Process Assumptions, especially on RC performance analysis for 10nm/7nm technology nodes. Due to continued CMOS scaling and larger process variations, Monte Carlo analysis has become necessary for RC performance estimation before matured hardware data is available for later model-to-hardware correlation.

Specific Responsibilities Include:

The intern will be responsible to find and verify the root cause of the ill-functional corner analysis of current closed-formed estimates of line resistance, and develop Monte Carlo analysis for line resistance and parasitic capacitance corners. The intern is expected to develop highly efficient Monte Carlo methodology through sensitivity study and appropriate regressions.

The intern will develop automatic generation of input files and programmable executions for finite element simulation (since tens of thousands of finite element simulations are needed; each run taking up to ten minutes).

The intern will have the opportunity to be immersed into state of the art of production processes for the latest CMOS technology nodes and new processes currently in research for future nodes. The intern is expected to determine statistical models and parameters from hardware to impact/contribute to true hardware representation in process assumptions.

Required Qualifications:

- Pursuing graduate degree majoring in Electrical, Computer, Mechanical Engineering or Physics, 2nd - 3rd year student preferred.

Additional Qualifications:

- Strong communication skills.
- Ability to collaborate and work in teams.
- Adaptability & flexibility.
- Good problem solving and knowledge of experimental methods.
- Planning & organization / able to drive and execute projects/work.